



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:) Art Unit: 2827
Fan et al.) Examiner: Jeremy C. Norris
Serial No.: 09/866,434) Date: December 11, 2002
Filed: May 29, 2001) Atty. Docket No. HCD-107
For: HIGH-RELIABILITY)
INTERPOSER FOR HIGHER-RISK)
PROCESSES)

A M E N D M E N T

Honorable Commissioner of Patents and Trademarks
Washington, DC 20231

S I R:

This amendment is responsive to the Office Action dated September 13, 2002 (Paper No. 4). Please amend the above-identified patent application as shown below.

IN THE DRAWINGS:

Please approve revised FIGURES 2, 3a, 3b, 5, 6a, and 6b, which applicants believe now show proper cross-hatching, and are herewith submitted as formal drawings.

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 4 with the following rewritten paragraph:

--This application is related to U.S. Patent No. 6,264,476, issued to Li et al. for WIRE SEGMENT BASED INTERPOSER FOR HIGH FREQUENCY ELECTRICAL CONNECTION, which is based on application Serial No. 09/457,776, filed December 9, 1999 and U.S. Patent No. 6,312,266, issued to Fan et al. for CARRIER FOR LAND GRID ARRAY CONNECTORS, which is based on U.S. patent application Serial No. 09/645,860, filed August 24, 2000, both of which are hereby incorporated by reference.--

IN THE ABSTRACT:

Please replace the abstract with the following rewritten abstract:

--An interposer provides a high reliability interface between an LGA connector and a motherboard. The interposer includes a stepped spacer for each solder interconnection which prevents the relaxation of mechanical contact force while ensuring the integrity of each solder interconnection.

The interposer provides noble metal plated contact pads on a

first surface to receive the contact members of an LGA connector, and contact pads for BGA solder connections for attachment to a motherboard. A description of the processes to manufacture the interposer is also disclosed.--

IN THE CLAIMS:

Please cancel claims 18 - 34, without prejudice. Please amend claim 1 as shown below.

1. (Amended) A low cost, high reliability interposer for use in electronic packages, comprising:

- a) at least one dielectric layer having one major surface and at least one edge;
- b) a plurality of conductive pads, each having a first and second surface, spaced apart on said major surface of said at least one dielectric layer, said first surface of said conductive pads being plated with at least one layer of metal, and at least a portion of said second surface of said conductive pads being readily adaptable for connection to a conductive member;

- c) a plurality of openings disposed in the interposer, said openings having a non-uniform cross section, each opening corresponding to and aligned with one of said conductive pads; and
- d) a plurality of reformable conductive members, each one located within one of said openings of said interposer and in electrical contact with said portion of said second surface of said conductive pads.

R E M A R K S

Reconsideration of the above-identified application is respectfully requested in view of the foregoing amendments and the following remarks. Applicants note Examiner Norris's restriction of claims 1 - 17 and 18 - 34 and hereby affirm the election of Group I, claims 1 - 17, by canceling claims 18 - 34 in the instant application. Claim 1 has been amended. Claims 1 - 17 remain in the case.

The specification has been amended in accordance with the Examiner's remarks regarding the abstract and to update related patent status. No new matter has been added.

Amendments to FIGURES 2, 3a, 3b, 5, 6a, and 6b are hereby proposed to include proper cross-hatching. For purposes of clarity, cross-hatching is shown on all non-conductive dielectric components. All un-shaded components are electrically conductive. No new matter has been added. Approval is respectfully requested.

This invention is an interposer that provides a high reliability interface between a land grid array (LGA) connector and a motherboard. The interposer overcomes the limitations of prior art interposers by including a stepped spacer for each solder interconnection which prevents the relaxation of mechanical contact force while ensuring the integrity of each solder interconnection. The interposer provides noble metal plated contact pads on a first surface to receive the contact members of an LGA connector, and contact pads for BGA solder connections for attachment to a motherboard.

Claims 1, 2, 10 and 12 - 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Desai et al. (U.S. Patent No. 5,880,590). While some aspects of DESAI appear similar to the present invention, there are significant differences. DESAI is an interposer to provide temporary connections between a flip-chip style chip having solder bumps or preforms and a ball grid array (BGA) chip carrier. The interposer is used for testing and burn-in of the chip while

avoiding distortion of the solder bumps or preforms and avoiding wear and damage to the BGA chip carrier.

As the Examiner points out, the embodiment in Fig. 1 of DESAI does show elements (a), (b) and (c), but the DESAI interposer does not have (d) a plurality of conductive members. In fact, DESAI's conductive members 42 are located on the semiconductor chip 40 and not as part of the low cost, high reliability interposer. The primary reason for the DESAI interposer is to keep the solder bumps on the chip and BGA chip carrier intact during chip test. This is significantly different from the interposer of the present invention, amended claim 1 of which includes deformable conductive members (e.g., solder balls) on the interposer that are intended to be deformed (i.e., reflowed) for at least semi-permanent attachment to a printed circuit structure such as a motherboard. The term "semi-permanent" is used to show that although the interposer is soldered to the motherboard, it may be removed from the motherboard (i.e., factory reworkable) if required. Since it is believed that the rejection of claim 1 of the present invention has been overcome, Applicants respectfully traverse the rejection of claims 1, 2, 10 and 12-17 under 35 U.S.C. §102(b) as being anticipated by DESAI.

Claims 1-3, 7, and 11-17 were rejected under 35 U.S.C. §102(e) as being anticipated by Haba et al. (U.S. Patent No.

6,428,328). HABA has several of the elements of the present invention, including "a plurality of conductive members" as in element (d) of claim 1. **The conductive members that HABA has on connector 102 are solder balls 126, and they are not located within the openings as recited in claim 1 of the present invention.**

Since HABA identifies element 102 as a microelectronic element connector and not as a reworkable interposer, there is a major functional difference between HABA and the invention. Moreover, conductive members 116 in HABA, "each one located within one of said openings and in electrical contact with said portion of said second surface of said conductive pads" are actually part of microelectronics 112 and not connector 102. HABA confirms these points in column 7, lines 39 - 45 and 52 - 61:

"The connector [!!] 102 is operative by means of the sockets 110 for connecting or mounting one or more microelectronic elements 112 [!!] overlying the top major surface 106. The microelectronic element 112 may be in the nature of a semiconductor chip, semiconductor chip package, a cable plug or other electronic element as is well known in the integrated circuit and semiconductor art....

"By mating the microelectronic element 112 with the top major surface 116 of the connector 102, the bump leads 116

will be received within the aligned sockets 110 so as to provide connection therebetween as to be described hereinafter. In this regard, the connecting of the microelectronic element 112 to the connector 102 will generally be characterized as a low or zero force insertion connection by virtue of the construction of the sockets 110 to be described".

The elements, the function, and the purpose of connector 102 of HABA all are different from the interposer of the present invention, especially since the interposer is "a high-reliability interposer for use in electronic packages" and is not a connector itself. Since it is believed that the rejection of claim 1 of the present invention has been overcome, Applicants respectfully traverse the rejection of claims 1-3, 7, and 11-17 under 35 U.S.C. §102(e) as being anticipated by HABA.

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over HABA in view of Green (U.S. Patent No. 6,219,253). GREEN shows means for preparing packaged electronic circuitry using molded plastics, Thick Film, and Build Up Technology, and achieving shielding of the circuitry and components of the package. There is no motivation in HABA to modify his patent with the teachings of GREEN; but even if there were such motivation, the addition of GREEN adding a plastic molding compound to an electronic package to

the teachings of HABA in no way anticipates, suggests or renders obvious Applicants' invention any more than does HABA alone. Since it is believed that the objection to claim 1 of the present invention has been overcome, Applicants respectfully traverse the rejection of claim 4 under 35 U.S.C. §103(a) as being anticipated by HABA in view of GREEN.

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over HABA in view of Brodsky et al. (U.S. Patent No. 5,984,691). BRODSKY shows a flexible circuitized interposer wherein the interposer includes at least one flexible circuitized substrate. There is no motivation in HABA to modify his patent with the teachings of BRODSKY; but even if there were such motivation, the addition of BRODSKY using polyimide as an insulative material in an interposer to the teachings of HABA in no way anticipates, suggests or renders obvious Applicants' invention any more than does HABA alone. Since it is believed that the objection to claim 1 of the present invention has been overcome, Applicants respectfully traverse the rejection of claim 5 under 35 U.S.C. §103(a) as being anticipated by HABA in view of BRODSKY.

Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over HABA in view of Bezama et al. (U.S. Patent No. 6,332,782). BEZAMA shows an interconnect substrate structure for electrical interconnection between two

electronic modules having differing conductive array parameters. There is no motivation in HABA to modify his patent with the teachings of BEZAMA; but even if there were such motivation, the addition of BEZAMA choosing an insulative material that has a CTE that matches the CTE of the surrounding structures for an interposer to the teachings of HABA in no way anticipates, suggests or renders obvious Applicants' invention any more than does HABA alone. Since it is believed that the objection to claim 1 of the present invention has been overcome, Applicants respectfully traverse the rejection of claim 6 under 35 U.S.C. §103(a) as being anticipated by HABA in view of BEZAMA.

Claims 8 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over DESAI in view of Babuka et al. (U.S. Patent No. 4,553,192). BABUKA shows an integrated circuit module to printed circuit board interconnection system wherein the board has circuit pads to which spring contacts have one of their ends soldered to the pads. It is clearly a connector as opposed to an interposer. There is no motivation in HABA to modify his patent with the teachings of BABUKA; but even if there were such motivation, the addition of BABUKA using multiple plating layers on conductive pads to the teachings of DESAI in no way anticipates, suggests or renders obvious Applicants' invention any more than does DESAI alone. Since it is believed that the objection to claim 1 of the present invention has been overcome,

Applicants respectfully traverse the rejection of claims 8 and 9 under 35 U.S.C. §103(a) as being anticipated by DESAI in view of BABUKA.

The Examiner also cited Gabrielian (U.S. Patent No. 4,029,375). GABRIELIAN shows a flat electrical connector employing axially compressed helical springs for contacts. The springs float in a housing between two flanking insulative members having printed circuit contact areas to mate with each end of each spring. GABRIELIAN does not show the interposer of the present invention, which is intended for use with an LGA connector.

The Examiner also cited Purinton (U.S. Patent No. 5,818,700). PURINTON shows an LGA connector. PURINTON does not show the interposer of the present invention, which is intended for use with an LGA connector.

The Examiner also cited Farnworth (U.S. Patent No. 5,893,765). FARNWORTH shows an LGA connector (with elastomeric members for the vertical interconnection) to provide the vertical interconnection from a die to the bonding pads on a semiconductor package. FARNWORTH does not show the interposer of the present invention, which is intended for use with an LGA connector.

The Examiner also cited Distefano et al. (U.S. Patent No. 6,044,548). DISTEFANO shows an LGA connector that is built on an interposer (Fig. 1 in DISTEFANO); in fact, Applicants have disclosed that interposer of that connector as prior art in FIGURE 3a of the present invention. Not only is DISTEFANO an LGA connector but it does not include the disclosed and claimed improvements of the interposer of the present invention.

In view of the foregoing amendments and remarks, Applicants respectfully request that claims 1-17 be allowed and the application be passed to issue.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

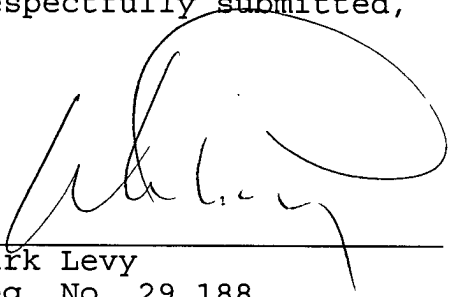
Respectfully submitted,

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Washington, D.C. 20231

On 12/12/02
(Date of Deposit)

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